New Product

N-Channel Reduced Q$_g$, Fast Switching MOSFET

PRODUCT SUMMARY

V$_{DS}$ (V)	r$_{DS(on)}$ (Ω)	I$_D$ (A)
30	0.0085 at V$_{GS}$ = 10 V	15
	0.0125 at V$_{GS}$ = 4.5 V	12

FEATURES

- TrenchFET® Gen II Power MOSFETS
- PWM Optimized
- 100 % R$_g$ Tested

RoHS
COMPLIANT

APPLICATIONS

- High-Side DC/DC Conversion
  - Notebook
  - Desktop
  - Server

SO-8

S 1   8 D
S 2   7 D
S 3   6 D
G 4   5 D

Top View
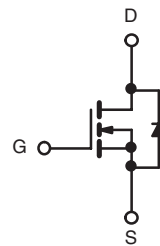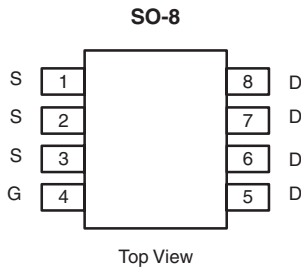
Ordering Information: Si4384DY-T1-E3 (Lead (Pb)-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T$_A$ = 25 °C, unless otherwise noted

Parameter		Symbol	10 sec	Steady State	Unit
Drain-Source Voltage		V$_{DS}$	30		V
Gate-Source Voltage		V$_{GS}$	± 20		
Continuous Drain Current (T$_J$ = 150 °C)[a]	T$_A$ = 25 °C	I$_D$	15	10	A
	T$_A$ = 70 °C		12	8	
Pulsed Drain Current		I$_{DM}$	± 50		
Continuous Source Current (Diode Conduction)[a]		I$_S$	2.8	1.3	
Single Pulse Avalanche Current	L = 0.1 mH	I$_{AS}$	25		
Avalanche Energy		E$_{AS}$	31		mJ
Maximum Power Dissipation[a]	T$_A$ = 25 °C	P$_D$	3.1	1.47	W
	T$_A$ = 70 °C		2	0.95	
Operating Junction and Storage Temperature Range		T$_J$, T$_{stg}$	- 55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET)[a]	t ≤ 10 sec	R$_{thJA}$	34	40	°C/W
	Steady State		71	85	
Maximum Junction-to-Foot (Drain)	Steady State	R$_{thJF}$	17	20	

Notes:
a. Surface Mounted on 1" x 1" FR4 Board.

MOSFET SPECIFICATIONS T_J = 25 °C, unless otherwise noted

| Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 70 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	40			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A		0.007	0.0085	Ω
		V_{GS} = 4.5 V, I_D = 12 A		0.0105	0.0125	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 15 A		56		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2.8 A, V_{GS} = 0 V		0.75	1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 15 A		12	18	nC
Gate-Source Charge	Q_{gs}			5.9		
Gate-Drain Charge	Q_{gd}			4.0		
Gate Resistance	R_g		0.8	1.7	2.5	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		10	15	ns
Rise Time	t_r			13	20	
Turn-Off Delay Time	$t_{d(off)}$			45	70	
Fall Time	t_f			13	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.8 A, di/dt = 100 A/µs		25	50	

Notes:
a. Pulse test; pulse width $\leq$ 300 µs, duty cycle $\leq$ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
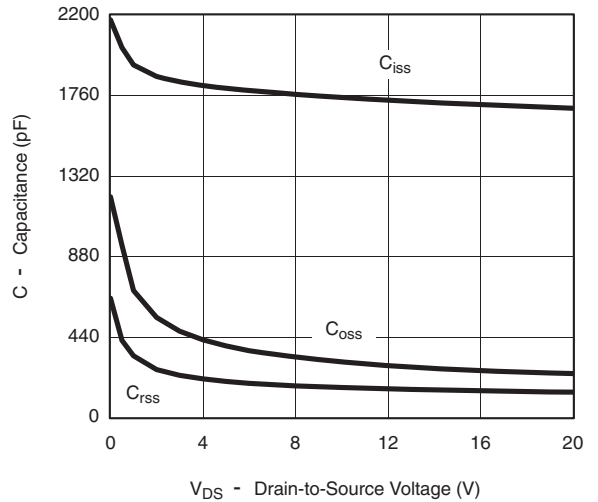
TYPICAL CHARACTERISTICS 25 °C unless noted

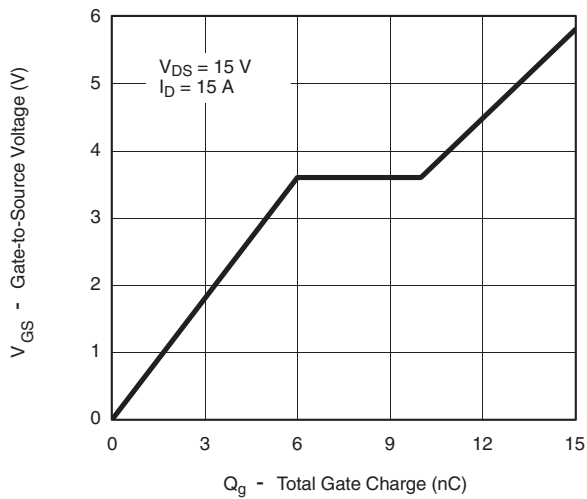**Output Characteristics**

Transfer Characteristics
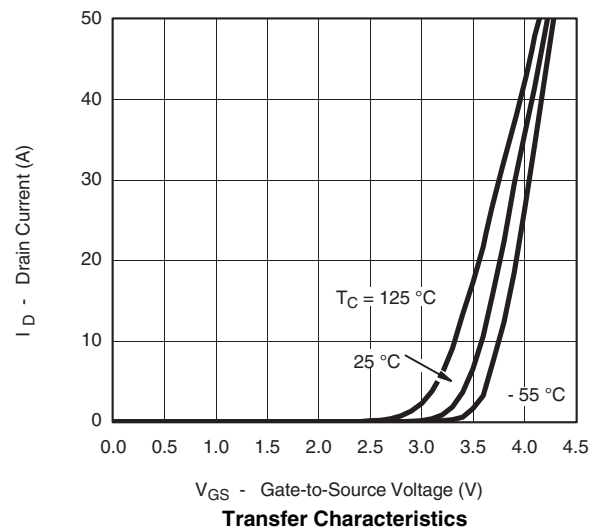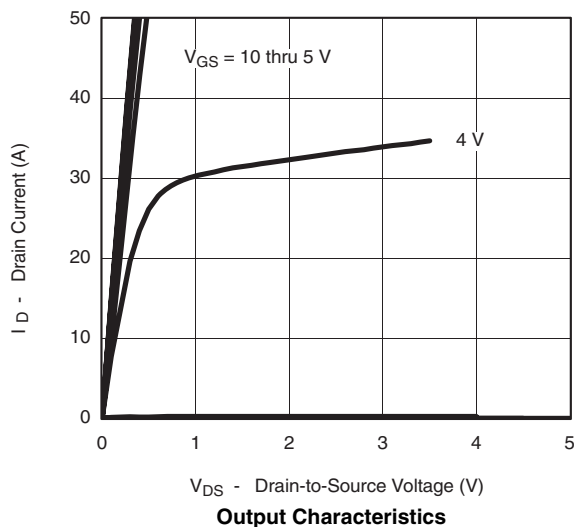
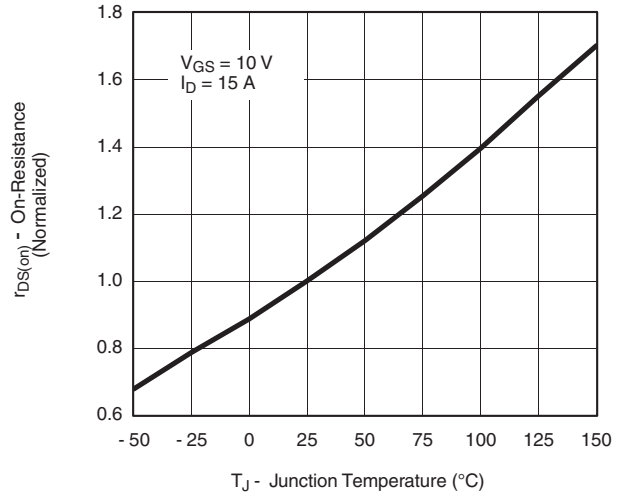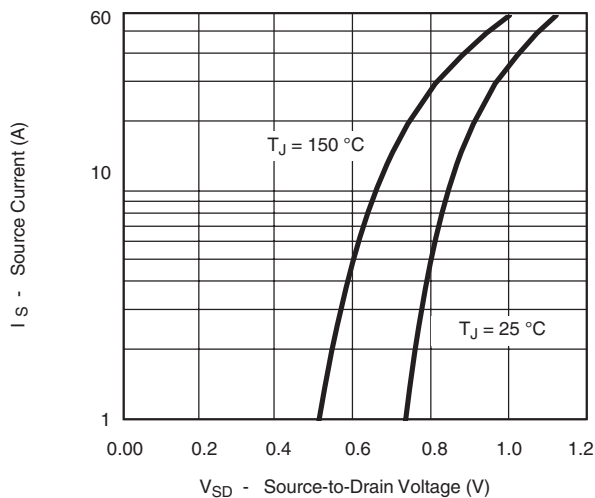## TYPICAL CHARACTERISTICS 25 °C unless noted
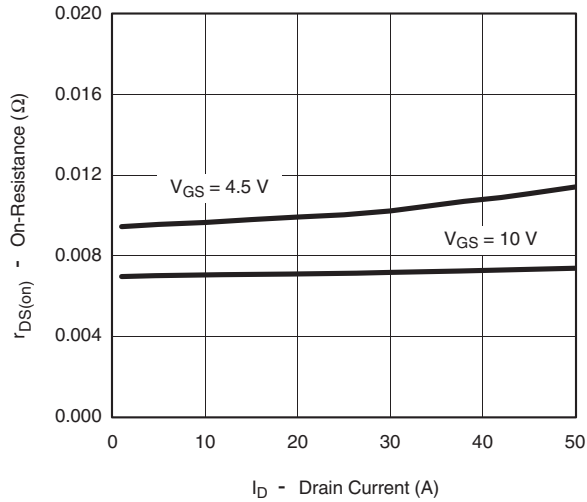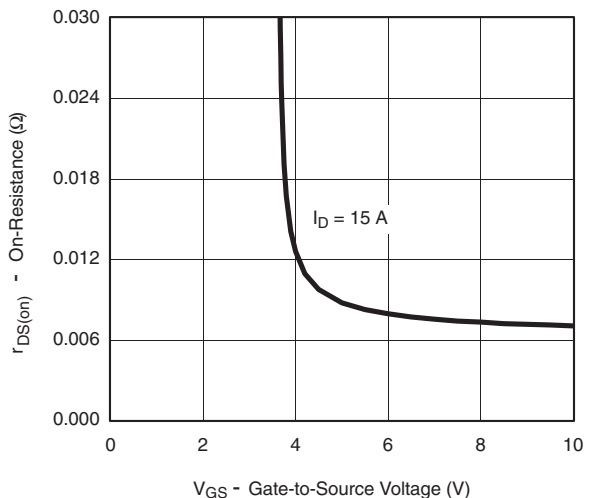
On-Resistance vs. Drain Current
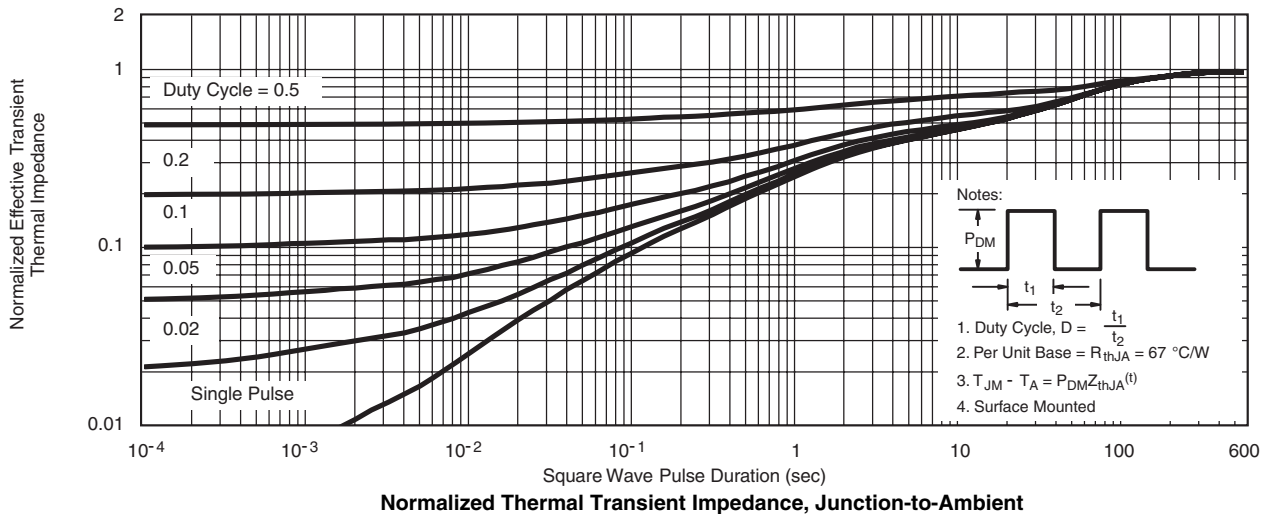
Capacitance
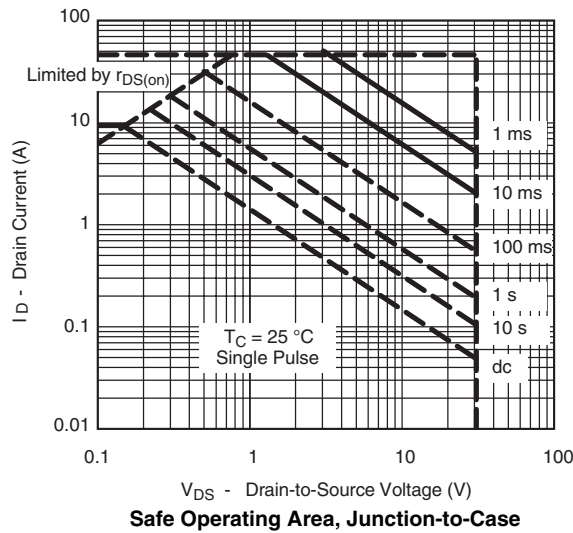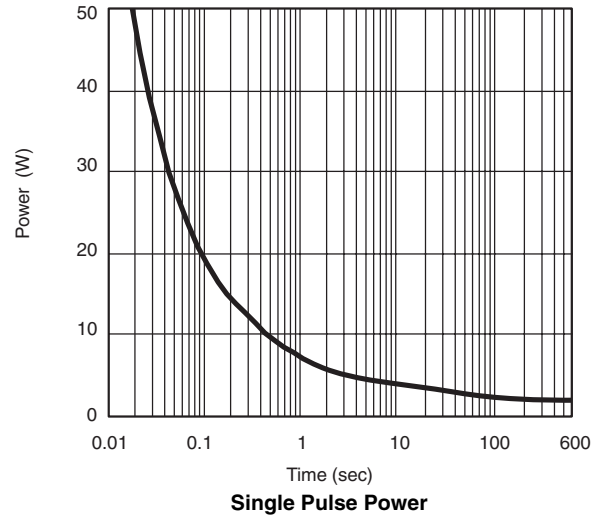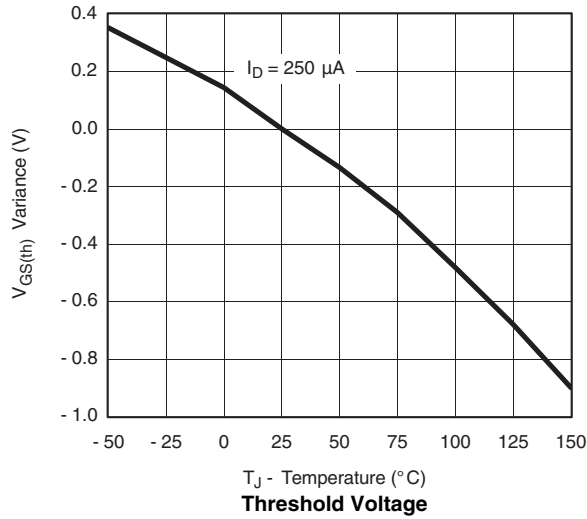
Gate Charge

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C unless noted

Threshold Voltage
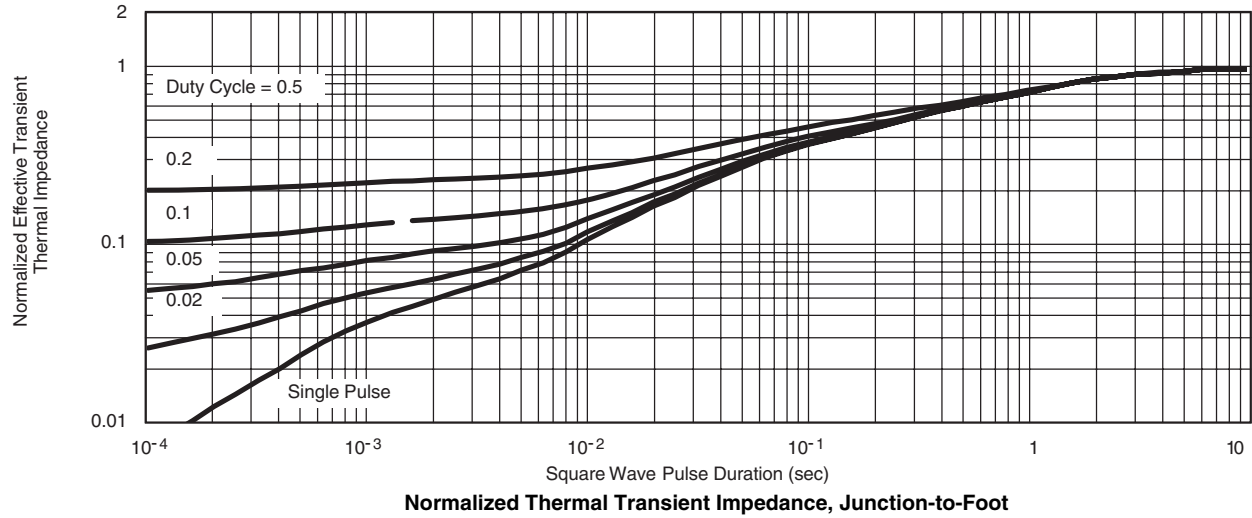
Single Pulse Power

Safe Operating Area, Junction-to-Case

Notes:
1. Duty Cycle, D = $\frac{t_1}{t_2}$
2. Per Unit Base = R_{thJA} = 67 °C/W
3. $T_{JM} - T_A = P_{DM}Z_{thJA}^{(t)}$
4. Surface Mounted

Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C unless noted

Normalized Thermal Transient Impedance, Junction-to-Foot

The chart shows "Normalized Effective Transient Thermal Impedance" (y-axis) vs "Square Wave Pulse Duration (sec)" (x-axis), with curves labeled Duty Cycle = 0.5, 0.2, 0.1, 0.05, 0.02, and Single Pulse.

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